ELEC50001 EE2 Circuits and Systems

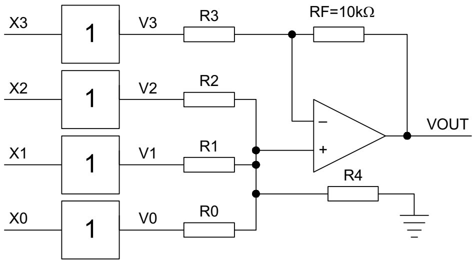
Problem Sheet 5 – Data Converters (*Lectures 8 and 10*)

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. A 3½ digit Digital Voltmeter has a display range of ±1999 and an accuracy of ±2 on the display. How many bits would a binary A/D converter need to have for its ±0.5 LSB accuracy to be as good as that of the DVM?

2B. A 12-bit converter has a resolution of 1 mV (i.e. 1 LSB = 1 mV) and input voltages in the range ±0.5 mV are converted to the value 0. What range of input voltages will be converted to –2047 ?

3B. A 10-bit converter converts an input voltage x to the value floor(x / 10mV). If 1 V < x < 8 V, what range of output values will be obtained ?



4C. X3:0 is a 4-bit signed number whose value, X, lies in the range –8 to +7. If the logic levels of V3:0 are 0 V and +5 V, choose values for R0 to R4 so that VOUT is equal to X/8 volts.

5C. The composite video signal to drive a monochrome TV monitor takes one of three different voltages according to the values of two digital signals DATA and SYNC:

DATA	SYNC	V_{OUT}
0	0	0.0
1	0	0.7
0	1	–0.3
1	1	Don't Care

Design a circuit to generate VOUT having a 50 Ω output impedance. You may assume that output logic levels are 0 and 5 V and that +5 V and –5 V power supplies are available should you need them. You do not need any op-amps although you will need at least one logic gate.

6B. Signals on a compact disc are stored as sequences of 16-bit numbers. Determine the maximum undistorted signal-to-noise ratio obtainable for a music signal whose peak amplitude is 10 times as great as its RMS value.

7C. A sample-hold circuit is used to store the input voltage of a 12-bit A/D converter during each conversion. The sample-hold circuit has an aperture uncertainty of 5 ns and a leakage current of ±1 nA. The A/D converter has an input voltage range of ±10 V.

If the input voltage is a sine wave of amplitude 10 V, calculate the input frequency at which the aperture uncertainty will result in an error of ±0.5 LSB [surprisingly low].

If the sample-hold uses a storage capacitor of 200 pF calculate how long the input voltage can be held before it changes by 0.5 LSB due to the leakage current.